



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/909,597	07/20/2001	Emiko Sekimoto	09792909-5093	3291

33448 7590 12/23/2003

ROBERT J. DEPKE LEWIS T. STEADMAN  
HOLLAND & KNIGHT LLC  
131 SOUTH DEARBORN  
30TH FLOOR  
CHICAGO, IL 60603

EXAMINER

GRAYBILL, DAVID E

ART UNIT PAPER NUMBER

2827

DATE MAILED: 12/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/909,597

Applicant(s)

SEKIMOTO, EMIKO

Examiner

David E Graybill

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 03 October 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

In the rejections *infra*, reference labels are generally recited only for the first recitation of identical claim language.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1, 3 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Arai (5686758).

At column 9, line 64 to column 10, line 62, Arai teaches the following:

1. A package for containing semiconductor element comprising:  
a housing 45 containing a semiconductor element, said housing having two primary side walls (illustrated, not labeled) that are perpendicular to each other; and a pair of positioning holes 53 and a pair of attaching holes 52 respectively provided at opposed side portions of said housing, wherein a line between said pair of positioning holes and a line between said pair of attaching holes intersect with each other substantially at a center of said package and further wherein the line between the positioning holes is skewed with respect to each of the two primary side walls of the housing and the line between the attaching holes is skewed with respect to each of the primary side walls such that the line between the positioning holes and the

line between the attaching holes are each neither parallel nor perpendicular to either of the primary side walls.

3. A semiconductor device comprising: a semiconductor element 40; a housing for containing said semiconductor element, said housing having two primary side walls that are perpendicular to each other; and a pair of positioning holes and a pair of attaching holes respectively provided at opposed side portions of said housing; wherein a line between the pair of positioning holes and a line between said pair of attaching holes intersect with each other substantially at a center of said package and further wherein the line between the positioning holes is skewed with respect to each of the primary side walls of the housing and the line between the attaching holes is skewed with respect to each of the primary side walls such that the line between the positioning holes and the line between the attaching holes are each neither parallel nor perpendicular to either of the primary side walls.

5. A semiconductor device comprising: a semiconductor element; a housing having a recess portion for containing said semiconductor element, said housing having two primary side walls that are perpendicular to each other; a pair of attaching holes provided at opposed side portions of said housing at a surface of said package; and a transparent member 48 for sealing said semiconductor element in said recess portion; wherein said surface of said housing is made to be higher than a top surface of said

transparent member, and further wherein a line between the pair of positioning holes and a line between said pair of attaching holes intersect with each other substantially at a center of said package and further wherein the line between the positioning holes is skewed with respect to each of the two primary side walls of the housing and the line between the attaching holes is skewed with respect to each of the primary side walls such that the line between the positioning holes and the line between the attaching holes are each neither parallel nor perpendicular to either of the primary side walls.

Note: The illustrated centerlines (not labeled) of Arai do not necessarily coincide with the instant claimed lines, and Arai is not necessarily relied on for the teaching of the illustrated centerlines.

Although Aria does not appear to explicitly teach wherein a line between said pair of positioning holes and a line between said pair of attaching holes intersect with each other substantially at a center of said package and further wherein the line between the positioning holes is skewed with respect to each of the two primary side walls of the housing and the line between the attaching holes is skewed with respect to each of the primary side walls such that the line between the positioning holes and the line between the attaching holes are each neither parallel nor perpendicular

to either of the primary side walls, these are inherent limitations of the package of Arai.

To further clarify, it is inherent that a straight or curved geometric element that is generated by a moving point and that has extension only along the path of the point, i.e., a line, can be generated between the positioning holes that is skewed with respect to each of the side walls of the housing, and it is inherent that a straight or curved geometric element that is generated by a moving point and that has extension only along the path of the point, i.e., a line, can be generated between the attaching holes that is skewed with respect to each of the side walls such that the line between the positioning holes and the line between the attaching holes are each neither parallel nor perpendicular to either of the primary side walls.

To additionally clarify, in Figures 4 and 6, it is inherent that a straight line can be generated between the positioning holes (symbolized but not labeled) that is skewed with respect to each of the side walls of the housing which are parallel to an x and y axis and a straight line can be generated between one pair of attaching holes (symbolized, not labeled) that is skewed with respect to each of the side walls which are parallel to an x and y axis.

To further clarify the teaching of a transparent member, the member inherently allows the passage of radiation; for example, infrared radiation, therefore, it is transparent at least to infrared radiation.

To further clarify the teaching that the surface of the housing is made to be higher than a top surface of the transparent member, it is noted that the scope of the claims is not limited to a particular frame of reference. In addition, the surface of the housing abuts and extends beyond a surface of the transparent member. Therefore, it is inherent that there is a frame of reference wherein the abutting surface of the transparent member is a top surface, and the further extending surface of the housing is made to be higher than the top surface.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2, 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arai as applied to claims 1, 3 and 5, and further in combination with Kondoh (5448114).

Arai does not appear to explicitly teach the following:

2. The package according to 1: wherein said semiconductor element is a solid-state imaging element.
4. The semiconductor device according to 3, wherein said semiconductor element is a solid-state imaging element.

6. The semiconductor device according to claim 5, wherein said semiconductor element is a solid-state imaging element.


Nonetheless, at column 3, lines 1-13, Kondoh teaches wherein a semiconductor element 1 is a solid-state imaging element, and a transparent member 21. Moreover, it would have been obvious to combine the product of Kondoh with the product of Arai because it would provide the semiconductor element of Arai and a transparent member.

Applicant's amendment and remarks filed 10-3-3 have been fully considered, and are adequately addressed in the rejections supra.

**Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.**

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947, or after about 02/05/04, (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is (703) 872-9306.

  
David E. Graybill  
Primary Examiner  
Art Unit 2827